REMARKS

Applicants submit a Petition and Fee for a One-Month Extension of Time.

An excess claim fee payment letter is submitted herewith for nine (9) total additional claims.

Claims 1-29 are all the claims presently pending in the application. Claims 1, 3-6, and 9 are amended to more clearly define the invention and claims 21-29 are added. Claims 1, 10, and 21 are independent.

These amendments are made only to more particularly point out the invention for the Examiner and not for narrowing the scope of the claims or for any reason related to a statutory requirement for patentability.

Applicants also note that, notwithstanding any claim amendments herein or later during prosecution, Applicants' intent is to encompass equivalents of all claim elements.

Applicants gratefully acknowledge that claims 10-20 are allowed. However, Applicants respectfully submit that all of the claims are allowable.

Applicants gratefully acknowledge that claims 3-9 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. However, Applicants respectfully submit that all of the claims are allowable.

Claims 1 and 2 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Yamashita et al. reference in view of the Korsh et al. reference.

This rejection is respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

An exemplary embodiment of the claimed invention, as defined by, for example,

independent claim 1, is directed to a display system that includes an array of pixel cells formed on a substrate. Each pixel cell is coupled to at least one gate line of a plurality of gate lines formed on the substrate and at least one data line of a plurality of data lines formed on the substrate. The device also includes a first and second transistor formed on the substrate. Each of the first and second transistors have a gate electrode and first and second electrodes defining a serpentine channel region there between.

Conventional display systems include pixel cells formed on a substrate which are each coupled to at least one gate line of a plurality of gate lines formed on the substrate and at least one data line of a plurality of data lines formed on the substrate. An array tester provides a means for testing the cells of such a display system by coupling probes to gate line pads and data line pads that terminate the gate lines and data lines, respectively. In other words, the array tester is coupled directly to each gate line and each data line. However, when the size of such a conventional display system is changed the spacing of the gate lines and/or data lines also changes which requires that the probe fixture of the array tester be modified to accommodate these changes.

By contrast, the present invention includes first and second transistors in addition to the pixel array which accommodate variations in size and/or resolution without requiring modification of the probe fixture of the array tester. In other words, the present invention provides a flexible interface between the array under test and the test system.

More specifically, in the event that the size of the array under test is changed, the gate line select/hold circuit 17 and/or the data line select/hold circuit 19 and the probe pads associated therewith may be designed such that they align with the spacing of an existing probe fixture, thereby eliminating the high costs associated with redesigning the probe fixture

of the array.

Further, each of the first and second transistors have a gate electrode and first and second electrodes defining a serpentine channel region. This feature minimizes the time constant required to transfer a charge to/from a capacitive load using the select and hold transistors of the gate line select/hold circuit 17 and the data line select/hold circuit 19 and also reduces the ON resistance of these transistors. The ON resistance of the transistor is proportional to the channel length/width ratio of the transistor. The serpentine channel region of each of these transistors minimizes this length/width ratio and, therefore, reduces the ON resistance and the time constant.

Exemplary embodiments of serpentine channel regions are illustrated by Figure 10(B) (marked up copy attached) and is described in the specification at, for example, page 20, line 20 - page 21, line 8. In particular, Figure 10(B) illustrates a serpentine channel region between electrodes A and C of the select transistor and another serpentine region between electrodes C and E of the hold transistor.

These serpentine channel regions along with their advantages were explained to Examiner Nguyen by the Applicants' representative during the May 13, 2004, personal interview.

II. THE PRIOR ART REJECTION

The Examiner alleges that the Korsh et al. reference would have been combined with the Yamashita et al. reference to form the claimed invention. Applicants submit, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Applicants submit that these references would not have been combined as alleged by the Examiner. Indeed, the references are directed to completely different and unrelated matters and problems.

Specifically, the Yamashita et al. reference is directed to providing an easy and reliable method of inspecting an active matrix substrate. (Col. 3, lines 17-21).

In stark contrast, the Korsh et al. reference is directed to the completely different and unrelated problem of reducing noise on a chip bus during output switching for a memory chip (col. 2, lines 16-19).

One of ordinary skill in the art who was concerned with providing an easy and reliable method of inspecting an active matrix substrate as the Yamashita et al. reference is concerned with providing would not have referred to the Korsh et al. reference, and vice-versa, because the Korsh et al. reference is directed to the completely different and unrelated problem of reducing noise on a chip bus during output switching for a memory chip. Thus, the references would not have been combined.

Further, the Examiner has failed to present a *prima facie* case for obviousness.

> *"To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art must teach or suggest all the claim limitations."* (M.P.E.P. § 2143).

In the present instance, the Examiner has failed to present a *prima facie* case for

obviousness because the Examiner has both failed to provide a suggestion or motivation to combine the teachings and has failed to provide prior art references that teach or suggest all the claim limitations.

The Examiner alleges that "It would have been obvious for one of ordinary skill in the art to provide (sic) substitute the transistors (sic) (2b) of Yamashita et al. (sic) for the transistor of Korsh et al. (sic) so that the current slew rate is reduced while the transistor is switching in order to reduce the occurred noise on the chip supply lines."

First, contrary to the Examiner's allegation the Yamashita et al. reference does not disclose "transistors (2b)." Rather, the Yamashita et al. reference discloses "a corresponding analog switch 2b." (See, for example, col. 4, lines 53-54). In other words, the Yamashita et al. reference only discloses a single transistor (switch) as corresponding to the reference numeral "2b" not more than one transistor such that it discloses "transistors (2b)" as alleged by the Examiner.

Second, the Examiner alleges that it would have been obvious to substitute the "transistors (2b) of Yamashita et al (sic) for the transistor of Korsh et al (sic)." The Examiner admits that the Yamashita et al. reference does not disclose a serpentine channel region. Therefore, to substitute the non-serpentine channel region transistor that is disclosed by the Yamashita et al. reference for the transistor that is disclosed by the Korsh et al. reference clearly would not provide a serpentine channel region as recited by the independent claims.

Third, the Examiner alleges that the Korsh et al. reference discloses "a transistor (as shown in figure 2) with . . . a serpentine channel region." The Examiner then alleges that it would have been obvious to combine the reference "so that the current slew rate is reduced

while the transistor is switching in order to reduce the occurred noise on the chip supply lines."

Of the references applied by the Examiner, only the Korsh et al. reference mentions anything at all that is even remotely related to reducing the current slew rate to reduce the noise. However, the Korsh et al. reference explains that the transistor illustrated in Figure 2 of the Korsh et al. reference suffers from the problems that the Examiner alleges are solved by the transistor of Figure 2 of the Korsh et al. reference.

In particular, the Korsh et al. reference explains that "conventional transistor construction for n-and p-channel transistors 10 and 12 is shown in Figure 2" and that "A problem with this conventional design is that the presence of unwanted and sometimes high voltage noise spikes on the Vcc and ground lines 14 and 16 of the chip whenever the output driver stage switches to a new state." (Emphasis added, col. 1, lines 25-52).

Therefore, contrary to the Examiner's allegation, it would not have been obvious to make the Examiner's alleged combination "so that the current slew rate is reduced while the transistor is switching in order to reduce the occurred noise on the chip supply lines" because the transistor construction that is disclosed in Figure 2 of the Korsh et al. reference clearly suffers from exactly that same problem that the Examiner alleges is solved by the combination.

Clearly, the Examiner has failed to present a *prima facie* case for obviousness because the Examiner has failed to provide a suggestion of motivation to combine the teachings as required by M.P.E.P. § 2143.

The Examiner has also failed to present a *prima facie* case for obviousness because the Examiner has failed to provide prior art references that teach or suggest all the claim

limitations.

In particular, the Examiner has again failed to apply any reference which teaches a serpentine channel region.

Before addressing the Korsh et al. reference directly, Applicants believe that a brief review of the fundamentals of the operation of a transistor is appropriate. The following description is based upon a description from *Introduction to Electronic Devices* by Michael Shur, 1996 by John Wiley & Sons, Inc, pg. 363, a copy of which is attached for the Examiner's convenience. An output current flows in a transistor between drain and source electrodes. This current is controlled by a gate bias. Depending upon the gate bias, a transistor can be either in the off-state, with very few free carriers in the transistor channel between the source and the drain, or in the on-state, when free carriers enter the transistor channel from the source and may flow to the drain. In the on-state, the free carriers in the transistor channel are capacitively coupled with the gate electrode, which effectively forms a parallel plate capacitor with the channel. The gate-to-channel voltage controls the free carrier charge induced into the channel and, hence, the drain current.

Therefore, since the current can only flow in a channel region due to the presence of a gate bias, a channel region can only be present where a gate is present.

Indeed, the Korsh et al. reference makes this very clear.

The Examiner alleges that the Korsh et al. reference discloses "first and second electrodes defining a serpentine channel region there between" in Figure 2.

However, contrary to the Examiner's allegation, the Korsh et al. reference clearly does not disclose any serpentine channel region.

Figure 2 of the Korsh et al. reference discloses a transistor construction having

"interlaced comb-like" source S and drain D electrodes with polysilicon gate electrode elements G passing between the source S and drain D elements to form a "comb-like" gate electrode. (Col. 1, lines 25-41).

The comb-like gate electrode G as illustrated by Figure 2 of the Korsh et al. reference provide a series of parallel, linear channel regions. As illustrated by the attached marked-up copy of Figure 2 of the Korsh et al. reference, the comb-like gate electrode G forms five separate and independent channel regions.

Figures 3 and 4 of the Korsh et al. reference illustrate this important distinction even more clearly.

Figure 4 of the Korsh et al. reference illustrates a "comb-like source electrode" formed by electrode elements 36a-e connected together in parallel to line 40, and electrode elements 38a-e that are connected together in parallel to an output pad 42 to form a "comb-like drain electrode" (col. 3, lines 56-61). "A polysilicon gate electrode 44 passes between the source and drain diffusion zones 32 and 34 in an elongated serpentine pattern with a plurality of reversals in direction." (Emphasis added, Col. 3, line 67- col. 4, line 2).

"This meandering gate pattern defines in effect a plurality of series-connected gate electrode elements 44a-e." (Emphasis added, Col. 4, lines 4-6).

"In effect, the transistor construction in FIG. 4 and shown schematically in FIG. 3 is that of a block of transistors N1, N2, . . . , in the present instance five transistors, connected with source in drains in parallel, but with series-connected gates." (Col. 4, lines 19-23).

In other words, as illustrated by the attached marked-up copy of Figure 4 of the Korsh et al. reference, the presence of five separate transistors 44a-e are defined by the presence of the gate electrode 44 between the source and drain regions 32 and 34, respectively. The

channel regions of the first four transistors 44a - d are U-shaped channel regions while the channel region of the fifth transistor 44e is a linear-shaped channel region.

The channel regions 44a - e do not form a serpentine channel region as claimed because the gate electrode 44 clearly diverts away from between the source and drain regions 32 and 34 to the area underneath the conductive line 40. In this manner, the channel regions 44a - e are only connected to each other such that they would form "series-connected gate electrode elements 44a-e" that provides "An RC delay line effect is produced by the series connection of the "resistors" R (the polysilicon gates) and shunt "capacitors" formed by the intrinsic gate capacitance." (Col. 4, lines 4-11).

Indeed, the Korsh et al. reference clearly teaches away from connecting these separate U-shaped channel regions 44a - e so that these "transistors of the present invention turn on sequentially beginning with transistor N1 nearest to the gate driver and ending with transistor N5 furthest from the gate driver." (Col. 4, lines 19-34).

Clearly, the Korsh et al. reference does not teach or suggest a serpentine channel region.

Rather, the Korsh et al. reference only discloses a serpentine gate electrode 44.

Lastly, the transistor construction suffers from the problems that are addressed by the present invention and which are solved by providing a serpentine channel region.

The Korsh et al. reference very clearly explains that the object is to reduce noise and that they address the problem of noise by forming an RC delay line using a "new transistor structure [that] is equivalent to a plurality of transistors with source and drains connected in parallel, with characteristic Z/L values that add up to the cumulative Z/L value of the prior art non-RC delay gate transistor structure, and with gates connected together in series to form the

RC delay line of the new transistor structure."

This "RC delay line causes the output transistor to turn on gradually, and reduces the output slew rate dI/dt noise by increasing the time it takes the output transistor to turn on." (Emphasis added, col. 2, lines 25-29). In other words, the Korsh et al. reference teaches increasing the time constant.

In stark contrast, the claimed invention provides a serpentine channel region which reduces the time constant. The serpentine channel region minimizes the amount of time required to transfer a charge to/from a capacitive load and also reduces the ON resistance of the transistors. The ON resistance of the transistor is proportional to the channel length/width ratio of the transistor. The serpentine channel region as recited by the claims reduces the channel length/width ratio and, therefore, reduces the ON resistance and the time constant.

This is in stark contrast to the teaching of the Korsh et al. reference which intentionally increases the RC delay line response so that "the RC delay line causes the output transistor to turn on gradually, . . ., by increasing the time it takes the output transistor to turn on." (Emphasis added, Col. 2, lines 25-29).

Clearly, the Examiner has not presented a *prima facie* case for obviousness.

Therefore, the Examiner is respectfully requested to withdraw the rejection of claims 1-2.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing amendments and remarks, Applicants respectfully submit that claims 1-29, all the claims presently pending in the Application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully

requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the Application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

Date: 10/8/04

James E. Howard
Registration No. 39,715

McGinn & Gibb, PLLC
8321 Old Courthouse Rd., Suite 200
Vienna, Virginia 22182
(703) 761-4100
Customer No. 48150

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Michael Shur

University of Virginia

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6

MOSFETs

6-1. PRINCIPLE OF OPERATION

The concept of a **Field Effect Transistor** (FET) was first proposed by Lilienfeld (1930). However, the device became practical only after pioneering work done by William Shockley in the early 1950s. Figure 6.1.1 shows the basic FET structure. An output current in a FET flows between the **drain** and the **source** contacts. This current is controlled by the **gate** bias. Depending on the gate bias, a FET can be either in the **off-state,** with very few free carriers in the transistor **channel** between the source and the drain, or in the **on-state,** when free carriers enter the transistor channel from the source and may flow to the drain. In the on-state, the free carriers in the transistor channel are capacitively coupled with the gate electrode, which effectively forms a parallel plate capacitor with the channel. The gate-to-channel voltage controls the free carrier charge induced into the channel and, hence, the drain current. Since the gate contact is isolated from the channel by the gate insulator, the input impedance is very high, a major advantage compared to Bipolar Junction Transistors.

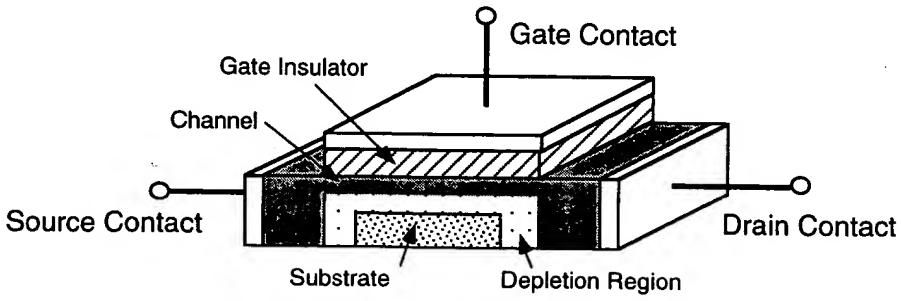

Fig. 6.1.1. Schematic illustration of a Field Effect Transistor (FET).

Field Effect Transistors use different semiconductors and different ways of

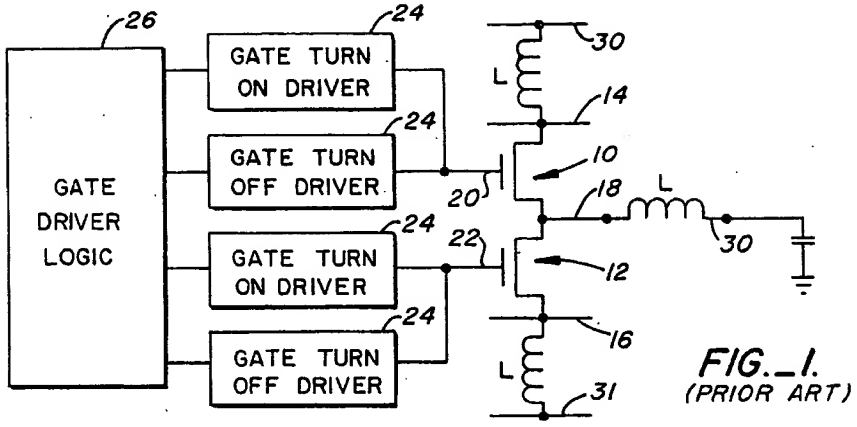

FIG._1.
(PRIOR ART)

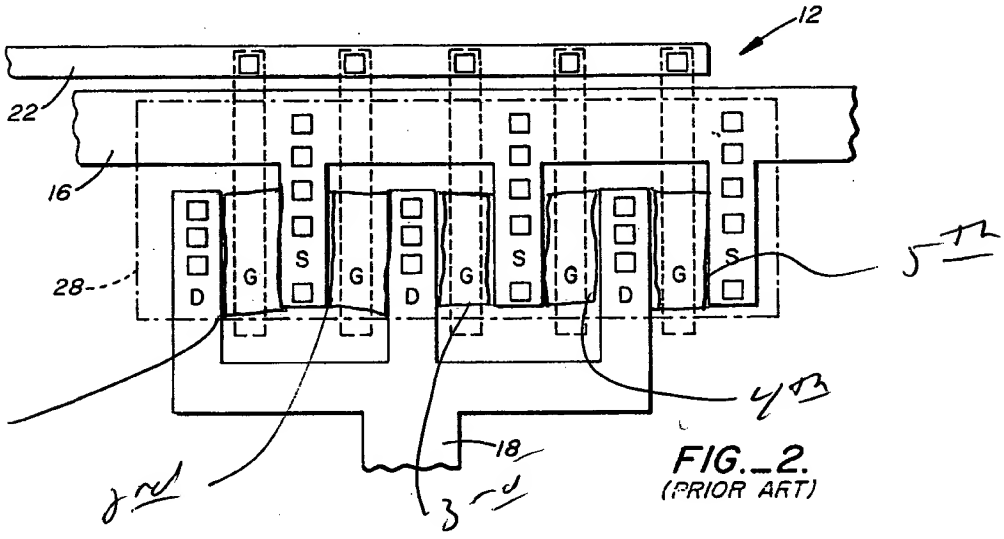

FIG._2.
(PRIOR ART)

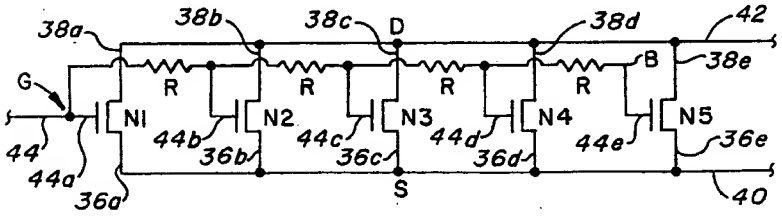

FIG._3.

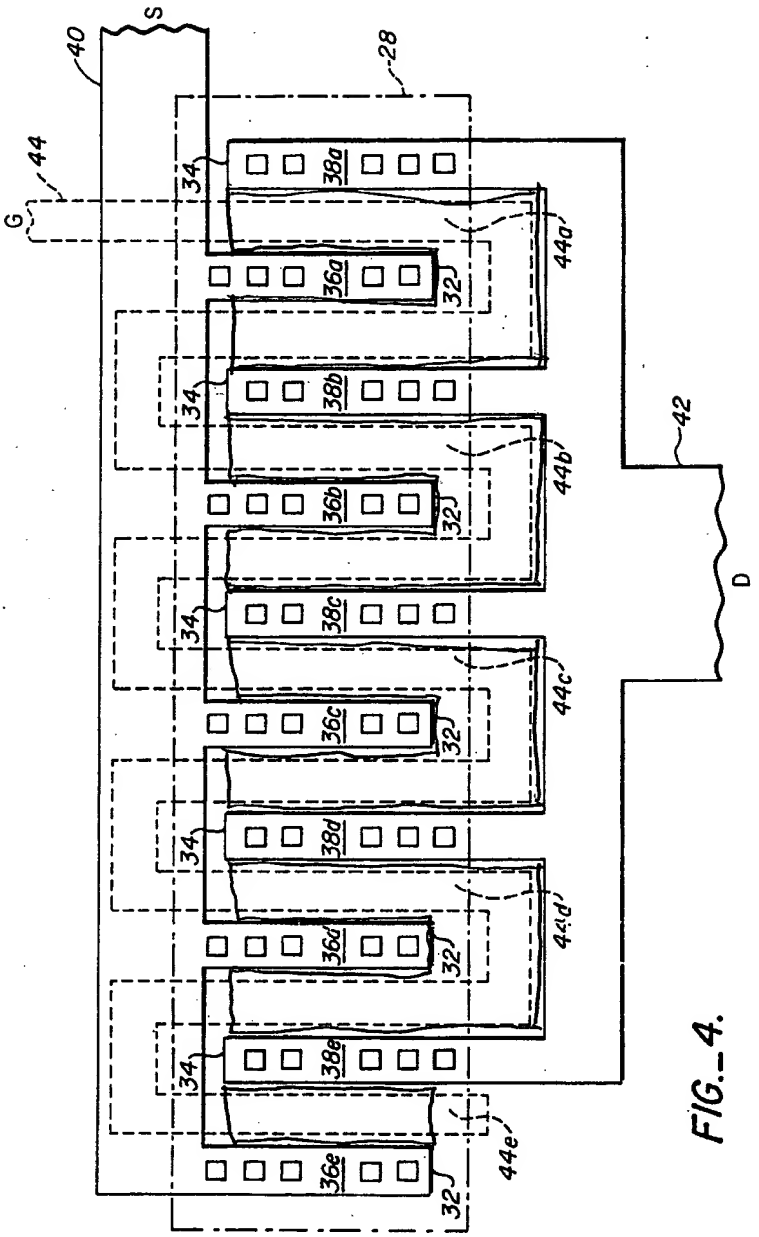
S
40
28
44
G
34
38a
36a
32
44a
38b
36b
42
44b
38c
36c
44c
38d
36d
44d
38e
36e
44e
D

FIG._4.

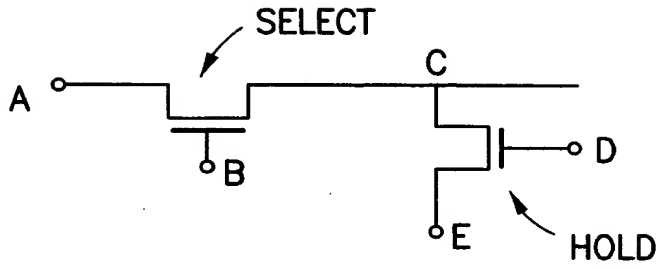

FIG.10(A)

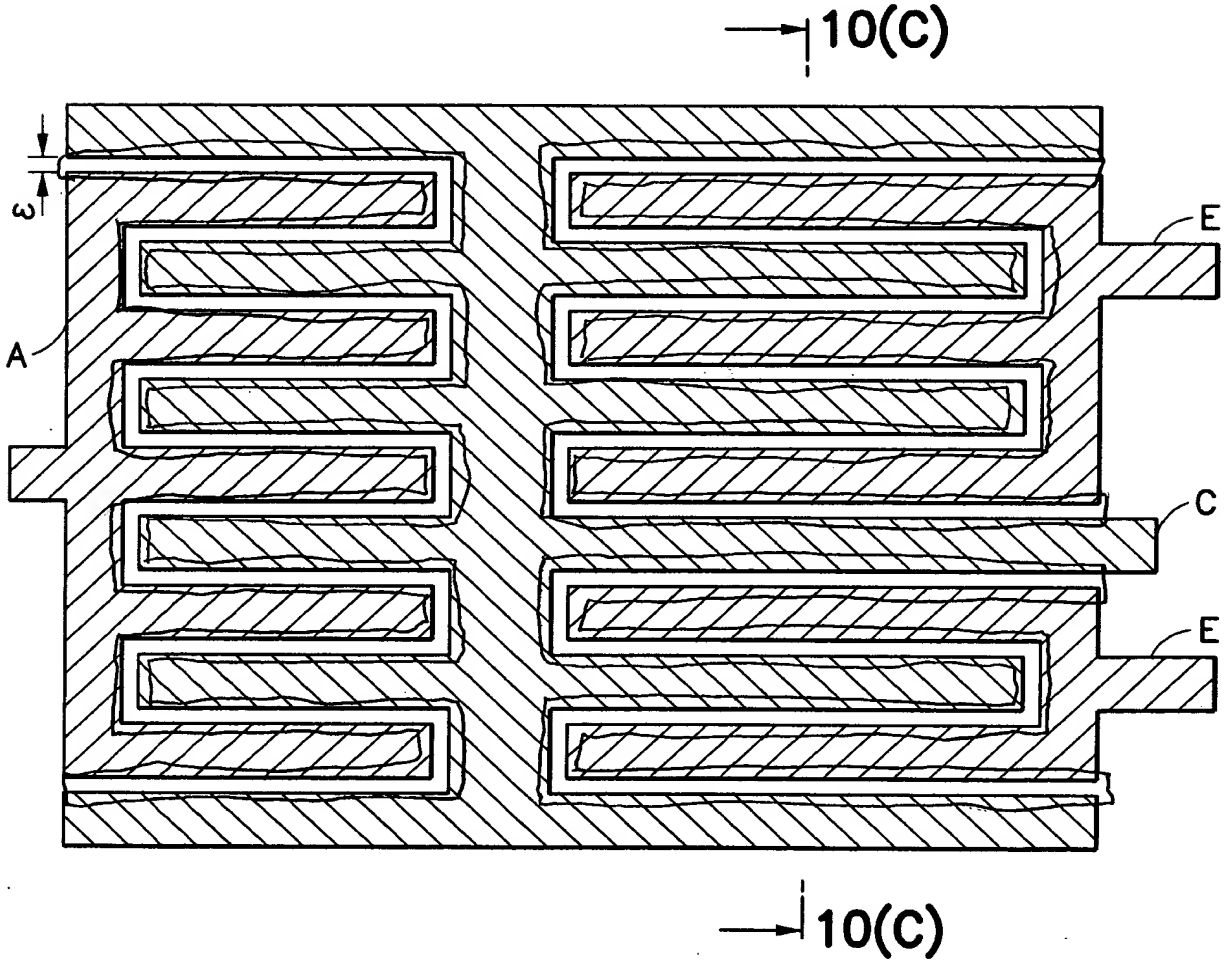

FIG.10(B)